Journal of Electroceramics, 13, 417–422, 2004

Fundamental Limits of Organic Packages and Boards and the Need for Novel Ceramic Boards for Next Generation Electronic Packaging

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Submitted March 4, 2003; Revised March 16, 2004; Accepted April 30, 2004

Abstract. The system-on-a-package (SOP) paradigm proposes a package level integration of digital, RF/analog and opto-electronic functions to address future convergent microsystems. Two major components of SOP fabrication are sequential build-up of multiple layers (4–8) of conducting copper patterns with interlayer dielectrics on a board and multiple ICs flip-chip bonded on the top layer. A wide range of passives, wave-guides and other RF and opto-electronic components buried within the dielectric layers provide the multiple functions on a single microminiaturized platform.

The routing of future nanoscale ICs with 10,000+ I/Os require multiple build-up layers of ultra fine board feature sizes of 10 μm lines/space widths and 40 μm pad diameters. Current FR4 boards cannot achieve this build-up technology because of dimensional instability during processing. These boards also undergo high warpage during the sequential build-up process which limits the fine-line lithography and also causes misalignment between the vias and their corresponding landing pads. In addition, the CTE mismatch between the silicon die and the board leads to IC-package interconnect reliability concerns, particularly in future fine-pitch assemblies where underfilling becomes complicated and expensive.

This work reports experimental and analytical work comparing the performance of organic and novel ceramic boards for SOP requirements. The property requirements as deduced from these results indicate that a high stiffness and tailorable CTE from 2–4 ppm/°C is required to enable SOP microminiaturized board fabrication and assembly without underfill. A novel ceramic board technology is proposed to address these requirements.

Keywords: FR4, electronic packaging, high density packaging, System-On-Package, Printed Wiring Board, SiC, flip chip, reliability, high density wiring

Introduction

The electronic systems which are primarily discrete currently are growing exponentially from 2 GHz to 20 GHz in digital and wireless performance and from Gigabit to Terabit per second in optical performance. The ICs are beginning to move to nano scale with 100 nm lithography, 100 million transistors, requiring more than 10,000 I/Os on 20–100 micron area array pitch and 200 watts of power. In addition, there is a strong trend toward so called convergent systems, converging data, voice and video by means of digital, RF, analog and optical functions in a single IC or microminiaturized board. Microsystems packaging serves as the bridge between ICs and systems. High density packaging (HDP) has a critical role in the microminiaturization of systems and has two major components; (a) IC packaging, and (b) systems packaging.

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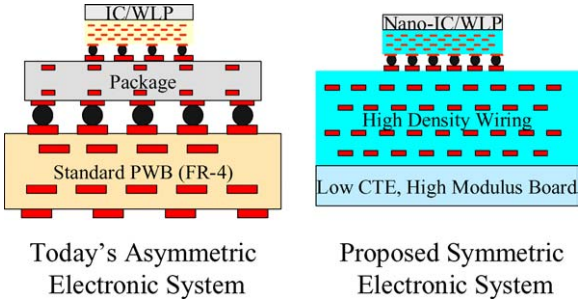

Fig. 1. Concept of future microminiaturized system-level packaging as opposed to today's discrete packaging.

High Density Packaging (HDP)

There is a critical need for a microminiaturized, multifunction board to realize the complex electronic systems of the future. This system board has to support extremely high wiring density with 4–8 layers of 5 μm wiring. Driven by miniaturization and high performance at the system level, area array packaging including flip chip will dominate the chip to the next level of interconnection for both the flip chip in package (FCIP) and direct chip attach (DCA) as well as wafer-level-packaging (WLP). For assemblies using flip chip attachment, a board that matches the routing requirements is needed. In other words, HDP is expected to move from today's asymmetric packaging to a highly integrated, symmetric concept involving a system micro board capable of interconnecting nano-ICs and also provide functions to compliment the ICs as shown in Fig. 1. However, one of the greatest challenges is the availability of organic boards capable of routing and interconnecting high I/O fine ICs.

Trends in Systems Packaging

Early system boards were large PWBs with 100 mil plated through hole technology. Advances in PWB materials and processes enabled the reduction of form factors and Plated-through Hole (PTH) sizes reduced to 10 mils in the 1980s and 90s. The advent of microvia technology with IBM's surface laminar circuitry (SLC) in the early 90s, enabled much higher systems integration and miniaturization. Embedded RF passives in the board will greatly enhance high frequency performance and reliability, and embedded optical waveguides will provide unprecedented data rates in system boards [1, 2]. Future systems will be built on highly integrated, microminaturized boards combining digital, RF and optical functions. Moving the on-chip global wiring onto the substrate using 5–10 μm board wiring is expected to reduce the wiring delay in digital systems [3].

There are four components to System-level packaging: (1) multifunction or microminiaturized board; and (2) wafer level SOC packaging, (3) 3-D IC packaging such as SIP; and (4) IC to board assembly.

Multi-Layered HDW Microvia Boards and Their Stiffness Requirements

Over the past few years, non-through hole vias and microvia technologies have played a key role in developing low cost and high density wiring (HDW) boards to accommodate the high I/O density of fine-pitch area-array packages such as flip chips and Chip Scale Packages (CSP). According to the Interconnect Technology Roadmap for Semiconductors (ITRS) for assembly and packaging, the projection for 2012 is to realize a microvia pad pitch of 50 microns with a pad size of 18 microns [4]. This system board has to support extremely high wiring density ($>$5000 cm/cm^2) with 4–8 layers of 5–15 microns of ultra-fine wiring and microvias for interconnections between multiple ICs.

The lack of dimensional stability in organic boards due to warpage is a serious technical barrier to achieve the fine-feature sizes required to meet the HDW roadmap requirements using conventional full-field UV lithography. The magnitude of the warpage depends on the following factors [5],

(i) The mismatch in thermomechanical properties.
(ii) The thickness of the base substrate and dielectric layers.
(iii) Curing temperature.

To systematically correlate the board warpage and HDW features, the effects of warpage are discussed with respect to two aspects. Firstly, the warpage prevents close contact between the mask and the board; hence the mask features cannot be accurately translated. Further, expansion and contraction between the various layers during the build-up process leads to layer-to-layer misregistration. This prevents microvias from landing on small capture pads in large area boards.

Warpage and Via-Pad Misalignment. The contribution to via-pad misalignment arises due to dimensional

changes of the board from the CTE mismatch between the build-up layers and the board. Assume that the distance between two microvias on the via-layer is L. The mask sets are designed such that the via and the top metal layers are in perfect alignment. The distance between the centers of the capture pad for the corresponding pads (on the metal layer masks) will also be L. When the via-mask is used to transfer and develop vias on the board, the distance between the two vias still remain L. However, after the board is cured at polymer dielectric cure temperature and cooled to room temperature, the distance between the two vias is no longer L but L-ΔL, where ΔL is the dimensional change experienced by the board from its stress-free dimension. Since the board's thickness and modulus is much higher than that of the polymer layer, the board determines the change in the linear dimension of the composite. Assuming that the capture pad at one end is aligned perfectly with the center of the underlying via, the capture pad center at the other end, at distance L, will be misaligned from its corresponding via by a distance of ΔL.

If $\varepsilon_{\text{board}}$ denotes the strain in the board, t_s is the board thickness and K is the board warpage expressed as curvature, the via-pad misalignment may be related to the curvature of the board as below [6].

$$\varepsilon_{\text{board}} = \frac{\Delta L}{L} = \frac{2}{3} t_s K$$

Thus, if a capture pad of 35 μm is used, the maximum board expansion, ΔL, that can be allowed across the largest dimension of the board (the diagonal) is 35 μm. The via-pad misalignment calculated from this method agrees with the experimentally measured via-pad misalignment on 3 candidate substrates, as shown in Fig. 2. For a board edge of 300 mm, the maximum board strain that can be tolerated is 35 micron/(300 mm $\times\sqrt{2}$). Substituting 0.85 mm and 1.2 mm for t_s, the board thickness for the hand-held sector and the cost-performance sector respectively, the maximum allowed warpage calculated from equation is 8.4 μm/inch for cost-performance applications and 12 μm/inch for hand-held applications after 200 μm build-up.

The maximum dimensional change in the board, ΔL that can be allowed across the board diagonal can be taken as the capture pad diameter. In other words, the maximum acceptable board warpage is directly proportional to the required capture pad diameter. If 20 microns pads are needed, the warpage limit further reduces to 4.75 microns/inch (for cost-performance) and 6.7 microns/inch (for hand-held) [4]. This makes solving via-pad misalignment a challenging issue because the maximum allowed board warpage has to be continuously lowered as the capture pad diameter decreases.

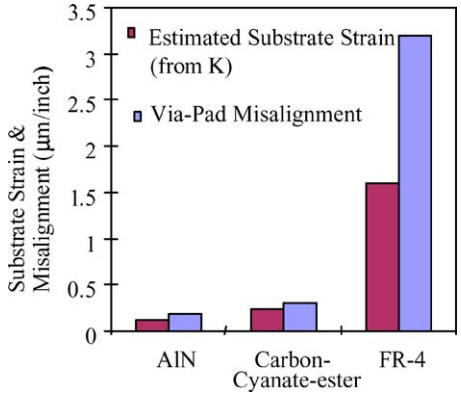

Fig. 2. Experimental and computed via-pad misalignments for a typical PWB sequential build-up process on 3 candidate boards.

Warpage and Mask Contact. To accurately define fine lines, the mask must make intimate or, hard contact with the board. Future build-up processes with ultra fine features (<15 μm) may require a glass mask. Unlike mylar masks, these masks do not conform to the board and hence the warpage induces gap between the board and mask. This gap has a substantial affect on the fine-line definition even for the one-layer build up studied here. The use of vacuum chuck has the effect of reducing the out-of-plane displacement of the board and possibly eliminating it for low values of warpage. Beyond certain threshold warpage and board stiffness, the gap between the board and the mask cannot be eliminated and leads to deterioration in the width of fine-lines. The average line width at the center can thus be correlated with the maximum out-of-plane displacement of each board.

From experimental work on fine line definition, it was seen that the line width significantly reduces with increase in the gap. When the gap is 50 μm, 100 μm lines on the mask result in less than 75 μm lines on the board resulting in 25% error in the line width. When the gap is more than 200 microns, the 100 microns line cannot be defined and the entire photoresist under the 100 μm line was exposed. A significant reduction in line widths was observed when a threshold warpage of about 4.6 μm/inch is reached.

Two upper specification limits for board warpage may be derived, one addressing fine lines and the other via-pad misalignment. Using these specfications,

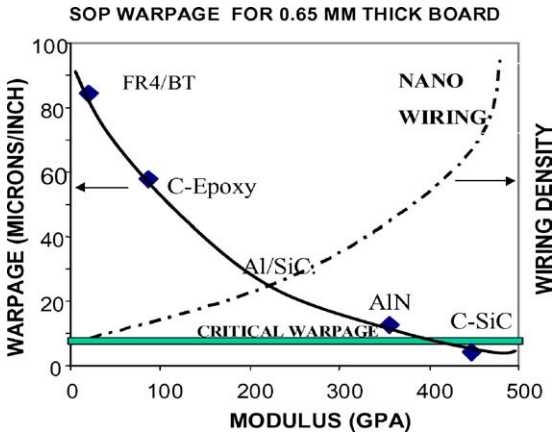

Fig. 3. Stiffness requirements to meet the experimentally derived threshold warpage for a typical SOP structure.

stiffness requirements can be derived for a particular multilayered structure. Figure 3 shows the warpage levels predicted for a SOP structure integrating RF front end with digital baseband (consisting of 12 build-up layers—8 for digital and 4 for RF) for different board materials and compares them to the upper specification limit for via-pad misalignment. All the layers are 8 microns thick except the RF inductor layer. The metal lines are 4 micron wide. For the hand-held sector with board thickness of 0.65 mm, the predicted warpage is higher than the warpage limit for all boards except C-SiC (450 GPa). For the cost-performance sector a stiffness higher than 350 GPa is desirable.

The results summarized in Fig. 3 show that FR-4 is not suitable for ultra fine feature sizes required in the future and underscore the need for stiffer ceramic-based board materials (>450 GPa) as replacement for FR-4. The lack of dimensional stability in organic boards due to moisture absorption and board warpage is a serious technical barrier to achieve the fine-feature sizes required for meeting the high-density wiring requirements. Since FR-4 has comparatively low stiffness, it is clear that it will not be flat enough to meet the above global interconnect requirements and hence should be replaced by materials with stiffness >450 GPa.

Board Property Requirements for Reliability of IC Assembly Without Underfill

The CTE mismatch between the board and chip is a major concern for the reliability of chip-board interconnects. FR4 and BT have CTE ranging from 15–18 ppm/C in comparison to Si (3 ppm/C). The expansion mismatch induces plastic strain in the solder joint during operation resulting in lower fatigue life. Though underfills are being adopted by the packaging industry to improve the reliability, they tremendously increase the assembly costs and assembly complexity. As such, they have not been widely adopted and pose major bottlenecks during the next-generation miniaturization. Warpage also limits fine-pitch chip assembly capabilities and reliability of interconnects. In order to attain the required reliability without underfill, the net CTE of the board has to tailorable, based on the number of high-density wiring layers that needs to built on it, to exactly match that of Si die (which has its own independent wiring).

Carbon fibers have negative CTE and high moduli, so their reinforcement in polymers seems to be a promising solution to get low CTE and moderate stiffness boards. These boards are relatively inexpensive and have easy machinability and large-area processability. In order to evaluate the suitability of carbon-epoxy boards to provide reliability without underfill, test vehicles were fabricated using conventional flip chip assembly. Continuous (unidirectional) and discontinuous carbon fiber reinforced epoxy composites, Si, AlN and FR-4 were used as base substrates for the test vehicle. An FR-4 test vehicle was used as a standard for comparison. To evaluate the increase in reliability performance of boards with CTE close to that of silicon, test vehicles were fabricated both with and without underfill. Reactive Ion Etching for better polymer adhesion initially roughened the substrates. Two different thicknesses of epoxy (CIBA 7081, Ciba-Geigy) were spin-coated on the substrate to provide the first insulation layer. Electroless copper plating was done using conventional PWB process and the copper wiring was subsequently electroplated up to 12 microns. The final solder mask coating was done with Taiyo solder mask composition. Bumped PB-8 dies (Flip-Chip Technology, Practical Components, CA) were assembled on the board with conventional flip-chip process both with and without underfill materials. A commercially available fast-flow, snap-cure underfill (Dexter 4531, Loctite Corporation) was used. Figure 4 shows the structure of test vehicle and process steps during the fabrication. Typical failure behavior is schematically shown.

Test vehicles were subjected to a thermal shock between -55°C to 125°C using liquid media. The thermomechanical reliability of the electrical interconnections was evaluated.

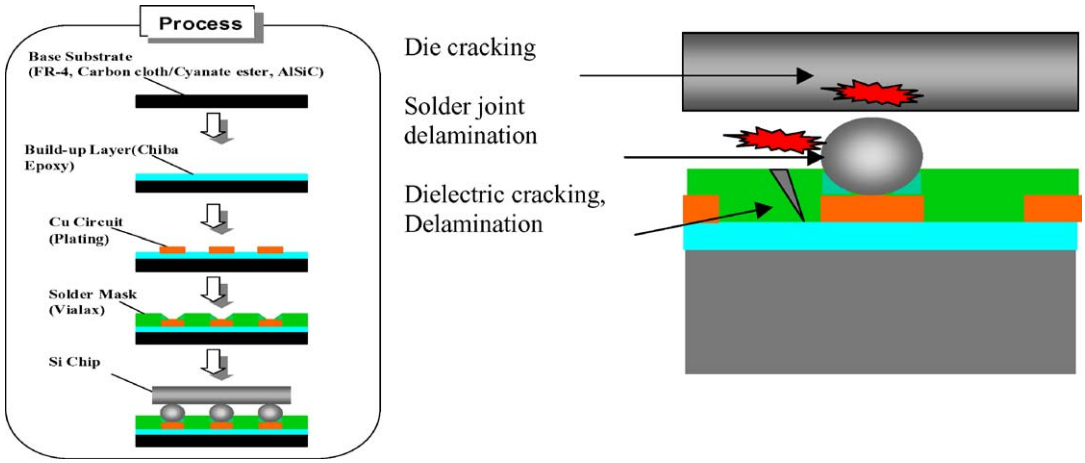

Fig. 4. Process flow for a flip chip assembly reliability test vehicle. Schematics of the failure criterion are also shown.

In order to understand the failure mechanisms, failure mode analysis was done using optical and scanning electron microscopy. Several types of failure modes namely solder joint cracking, solder joint delamination, dielectric cracking, underfill, and die cracking were observed in the test vehicles. Conventional base substrate material FR-4 has been observed to fail within the first 100 cycles without underfill. As expected, the failure occurred at the solder joints due to the huge CTE mismatch between the Si die and the board. Test vehicles with underfill have been observed to sustain up to 1800 cycles as the underfill redistributes the stresses in the solder joints. Test vehicles built on low CTE substrates with low modulus (∼100 GPa) fail at early stages of thermal cycle, both with and without underfill. Both dielectric cracking and solder joint delamination were observed in the test vehicles. The low CTE results in a large CTE mismatch between the dielectric and board which generates high stresses in the dielectric causing it to crack. In addition, the low stiffness causes the boards to warp during thermal cycling leading to solder joint delamination. The cracks in the dielectric propagate into the copper lines breaking the electrical continuity and thereby leading to failure of the assembly (Fig. 5).

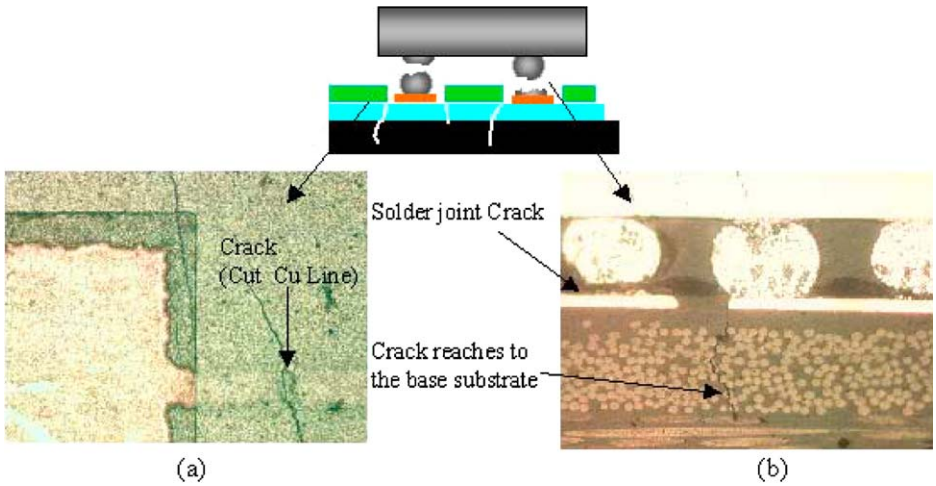

Fig. 5. Failure analysis of flip chip assembly on low-CTE carbon-epoxy boards.

It is important to notice that for the carbon cloth reinforced epoxy substrate, reliability is quite low though effective CTE mismatch between the die and the board has been eliminated.

The unidirectional carbon—epoxy boards and silicon with a higher modulus (∼180 GPa) show similar failure modes though they fail at a later stage than board A, both with and without underfill. AlN, which is a low CTE-high stiffness (350 GPa) board, has good reliability both with and without underfill and does not fail even after 1800 cycles. It was also seen that the boards with lower thickness of dielectric could pass through greater number of cycles before failure. Aluminum nitride with a CTE of 4 ppm/C and stiffness above 300 GPa did not fail both with and without underfill. While the dielectric stresses on AlN board are expected to be similar to that on low-CTE carbon-epoxy boards, the AlN test vehicle did not show any dielectric cracking presumably because of the low in-situ warpage during thermal cycling. A combination of high dielectric stress and cyclic warpage seems to have resulted the cracking in the low-CTE low-stiffness boards. Hence, it is critical for the low-CTE board material to have sufficient stiffness to prevent dielectric cracking from cyclic warpage. From both the processing and reliability analysis, it is important that the board has sufficiently high stiffness.

The cost targets dictated by ITRS/NEMI roadmaps [7] require that the board technology and material to be processable in large-area so that it can be processed similar to organics to yield the economies of scale. The above analysis also shows that the boards should have the mechanical stability and performance of ceramics to support the fine-feature geometries with high reliability. Materials such as AlN are not easily processable in large-area and are quite expensive. Hence, novel high stiffness ceramic-based low CTE board materials that are processable in large-area need to be developed to meet the future packaging requirements. Powder technology cannot achieve large-area manufacturability (12 inch to 18 inch) at low cost. Polymer Derived Ceramic (PDC) technology can be ideal for these applications. C-SiC composites derived from preceramic polymer and high-stiffness carbon cloth appears to be an ideal candidate material that satisfies all the above properties and is currently being explored.

Summary

This work examines the property requirements for board materials that meet the microminiaturized systems packaging requirements of the future. Two barriers are identified for the current organic based board materials—lack of board dimensional control because of warpage and distortion during the sequential build-up process and the CTE mismatch between the board and IC which necessitates the use the underfill materials. Analytical modeling and experimental studies indicate that ceramic-based board materials with ultra-high modulus and tailorable low CTE are required to meet the required microvia/pad, line/spacing requirements and achieve fine-pitch interconnect reliability without underfill.

Acknowledgments

The authors wish to thank the National Science Foundation (grant number EEC-9402723), its industry partners for their support, and all PRC faculty, National Institute of Standards and Technology (NIST-ATP), students and research staff for their contributions to this work.

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